FIG. 31 (A) is a plan view of another kind of the power source plain layer 16P in the inner layer in FIG. 22 and FIG. 31 (B) is a plan view of the grounding plain layer 16E in the inner layer;

FIG. 32 is a graph indicating the quantity of the through holes having no dummy land, with the quantity of the through holes having no dummy land on the abscissa axis and the value (V) of the voltage drop amount on the ordinate axis;

FIG. 33 is a table showing the relation between the thickness of the conductor in the inner layer and the voltage drops of the first time to third time;

FIG. 34 is an explanatory diagram showing the relation between the through hole and the conductive layer;

FIG. 35 is a sectional view of the multilayer printed wiring board according to a related art of the present invention;

FIG. 36 (A) is a lateral sectional view taken along X4-X4 of the multilayer printed wiring board of FIG. 35 and FIG. 36(B) is a sectional view taken along X5-X5;

FIG. 37(A) is a plan view of the power source plain layer 16P in the inner layer and FIG. 37(B) is a plan view of the grounding plain layer 16E in the inner layer;

FIG. 38 is a lateral sectional view of the multilayer printed wiring board of a conventional technology;

FIG. 39 is a schematic view of the signal through hole passing the multilayer core; and

FIG. 40 is a graph showing the amounts of voltage drops of the first time and second time.

BEST MODES FOR CARRYING OUT THE INVENTION

A.EMBODIMENT 1

[EMBODIMENT 1-1]